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## (54) Apparatus for computing power consumption of MOS transistor logic function block

Gerät zur Berechnung der Leistungsaufnahme eines aus MOS-Transistoren zusammengesetzten Logik-Funktionsblocks

Dispositif pour calculer la consommation de puissance d'un bloc de fonction logique à transistors MOS

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## Description

**[0001]** This invention relates to an apparatus for computing power consumed by a semiconductor circuit including a plurality of macrocells including MOS transistors, and more particularly to. apparatus for computing power consumption caused by "through-current" which flows through macrocells.

**[0002]** A macrocell is a circuit, such as a NAND circuit and an OR circuit, or a combination of such circuits, which can perform functions desired by a user. A term "through-current" as used herein is defined as follows. For example, in a circuit including a series combination of an N-type MOS transistor (hereinafter referred to as NMOS transistor) and a P-type MOS transistor (hereinafter referred to as PMOS transistor), when, for example, the PMOS transistor changes from a nonconductive state to a conductive state and the NMOS transistor changes from a conductive state to a nonconductive state, both transistors may become conductive for some time due to difference in threshold between the PMOS and NMOS transistors. Current which flows through these two conductive transistors is called "through-current". In MOS transistor macrocells, such MOS transistor series circuits are frequently used, which often causes through-current to flow.

**[0003]** Power consumption in semiconductor circuits comprising macrocells when they are operating is computed in order to estimate power consumption to avoid troubles in the semiconductor circuits, such as degradation of performance of the circuits. In such computation, it is necessary to first compute power consumption in each of macrocells. Power consumption in a macrocell includes power consumption due to through-current and power consumption due to charging and discharging of load capacitance of macrocell.

**[0004]** FIGURE 1 is a block diagram of an apparatus for computing power consumption in one macrocell. The computation is carried out based on the results of logic simulation on a semiconductor circuit including that macrocell. In FIGURE 1, circuit information deriving means 1 identifies a macrocell which has operated from data 2 relating to input/output signal variations in the logic simulation, names of macrocells, and a net list 3 storing information relating to how that macrocell is connected to other macrocells, and then derives the load capacitance of that macrocell as circuit information from load capacitance data 4.

**[0005]** Fixed-value storage means 5 stores a fixed value for each macrocell representing power consumption Wp due to through-current in that macrocell as determined by applying a suitable input waveform and providing predetermined output load capacitance to that macrocell.

**[0006]** Through-current power consumption Wp determining means 6 reads out power consumption Wp caused by through-current in a macrocell specified by circuit information deriving means 1 from fixed-value storage means 5.

**[0007]** Load-capacitance power consumption Wc determining means 7 computes power consumption Wc caused by charging or discharging of the load capacitance of a macrocell specified by circuit information deriving means 1. That is, means 7 computes the power consumption Wc according to well-known expressions for power consumption caused by load capacitance.

**[0008]** Summing means 8 sums the power consumption Wc and the power consumption Wp.

**[0009]** The above-described apparatus is for computing power consumption in one macrocell, but usually it is also necessary to compute overall power consumption of the semiconductor circuit formed of such macrocells.

**[0010]** For that purpose, as shown in FIGURE 2, means 9 for identifying the macrocells which have operated identifies the names of the respective macrocells having input/output signal changes in logic simulation, based on information from logic simulation result storage means 10 and net list 3. Means 9 also derives the number of operation cycles per unit time.

**[0011]** The data is fed to means 12 for deriving therefrom power consumption W1, W2, ..., Wn in respective macrocells, as in the power consumption computing apparatus of FIGURE 1, to compute power consumed in each cycle of operation of the respective macrocells (including power consumption due to through-current and power consumption due to load capacitance). In this example, the identification of macrocells which have operated is performed by means 9.

**[0012]** The thus computed power consumptions in the respective ones of macrocells are summed in summing means 13 which sums power consumption W1, W2, ..., Wn. From the number of times the respective macrocells which have been identified by means 9 as having operated, the power consumption per unit time of each macrocell is determined. For example, if a macrocell have operated three times in a unit time period, the power consumed by that macrocell in the unit time period is computed by multiplying the power consumed in one operating cycle by the number of operating cycles, three in this case. Power consumed in the unit time period in other macrocells which have been identified as having operated is computed. The power consumption is summed to produce overall power consumption in the entire semiconductor circuit.

**[0013]** In Japanese Unexamined Patent Publication No. HEI 2-171861 (JP-A-21 71 861), a system for computing power consumption in a CMOS gate array is disclosed. According to the teaching of this Japanese patent publication, power consumption is computed from data relating to variations in input/output signal to and from the respective macrocells of the circuit, data to load capacitance and so forth. The technique shown therein first computes an operating frequency of a macrocell of interest from the input/output signal variations and, then, uses it in computing the power

consumption. When the macrocell is a NAND circuit, the power consumed by the macrocell is determined by the product of the output frequency, the load capacitance and the power consumption factor inherent to that NAND circuit. If the macrocell is a D-type flip-flop, the power consumed by the macrocell is the sum of the input signal frequency multiplied by the power consumption factor of the flip-flop and the output frequency multiplied by the load capacitance and the power consumption factor. Such computation is similar to the computation of power consumption due to load capacitance in unit time of one macrocell shown in FIGURE 1 or 2. This prior art does not take power consumption caused by through-current into consideration.

**[0014]** Since power consumption caused by through-current is not taken into consideration in this prior art technique, power consumption cannot be computed precisely. In the systems shown in FIGURES 1 and 2, power consumption due to through-current is taken into consideration, but it is treated as a fixed value. Therefore it is impossible to compute power consumption precisely.

**[0015]** Actual through-current is dependent on the slope of a input signal waveform applied to a macrocell, and shift of operating points of MOS transistors of the macrocell caused by changes in charge and discharge current for an output side load capacitance of the macrocell, and, therefore, power consumption Wp due to through-current is not constant. (Hereinafter, the above-stated slope of input signal waveform is referred to as input slew rate or slew rate.)

**[0016]** TABLE 1 shows the result of simulation for power consumption caused by through current in a macrocell, e. g. NAND circuit.

TABLE 1

| Load \ Slew Rate | 1.0 | 2.0 | 3.0 | 4.0 | 5.0 |
|---|---|---|---|---|---|
| 0.2 | 2.05 | 3.14 | 4.42 | 5.78 | 7.18 |
| 0.4 | 2.02 | 2.96 | 4.11 | 5.38 | 6.70 |
| 0.6 | 2.00 | 2.82 | 3.89 | 5.07 | 6.33 |

**[0017]** TABLE 1 shows the result of simulation performed on a NAND circuit 40 shown in FIGURE 3. NAND circuit 40 comprises two PMOS transistors 41 and 42 having their drain-source conduction paths connected between a +5V voltage supply terminal and an output node Y, and also two NMOS transistors 43 and 44 having their drain-source conduction paths connected in series between output node Y and a point of reference potential. The gates of PMOS transistor 41 and NMOS transistor 43 are connected to an input terminal A, and the gates of PMOS transistor 42 and NMOS transistor 44 are connected to an input terminal B. Computation of power consumption in this circuit has been made on the assumption that input terminal A is fixed to, for example, +5V and voltage change from +5V to 0V is applied to input terminal B. More specifically, initially, both input terminals A and B are at +5V and, accordingly, both of NMOS transistors 43 and 44 are conductive, whereas both of PMOS transistors 41 and 42 are nonconductive. Therefore the voltage at output node Y is 0V. When the voltage at input terminal B starts changing from +5V toward 0V, there will appear a time period during which PMOS transistor 42 and NMOS transistors 43 and 44 are all conductive, because the threshold voltage at which PMOS transistors change from nonconductive to conductive states is higher than the threshold voltage at which NMOS transistors change from conductive to nonconductive states. After that time period, NMOS transistor 44 becomes nonconductive so that output node Y becomes +5V. Current which flows through PMOS transistor 42 and NMOS transistors 43 and 44 during the time period when these transistors 42, 43 and 44 are all conductive is "through-current".

**[0018]** In TABLE 1, "Slew Rate" is an input slew rate expressed in terms of nanosecond (ns), and "Load" is an output load capacitance in pico-farad (pF). In this example, the slew rate is a function of an input-side overall capacitance cl at terminal B, which is determined by the gate capacitance of each of NMOS and PMOS transistors 44 and 42, capacitance provided by metal conductors for connecting input terminal B of NAND circuit 40 to a macrocell in the preceding stage, for example, a similarly arranged NAND circuit 40a, and drain capacitance of each of MOS transistors of NAND circuit 40a corresponding to PMOS transistor 42 and NMOS transistors 43 and 44. An output-side capacitance c2 is determined by drain capacitance of each of PMOS transistor 42 and NMOS transistors 43 and 44 of NAND circuit 40, capacitance of wires for connecting NAND circuit 40 to a succeeding macrocell, e.g. an NAND circuit 40b similar to

NAND CIRCUIT 40, and, further, the gate capacitance of each of MOS transistors of NAND circuit 40b corresponding to PMOS transistor 42 and NMOS transistor 44 if output node Y is connected to input terminal B of NAND circuit 40b. The reason why load capacitance c2 and input-side overall capacitance cl as represented by "Slew Rate" have various values as shown in TABLE 1 is that because the positions of NAND circuits used as NAND circuits 40a and 40b relative to NAND circuit 40 are not fixed due to circuit design, the lengths of metallic wires change accordingly.

**[0019]** From TABLE 1, it is seen that in response to changes in slew rate and output-side load capacitance, power consumption in NAND circuit 40 varies in a range of from 2.00 to 7.18 μ W/MHz. However, while the actual power consumption is variable as shown, prior art uses one fixed value within this variation range, e.g. a true value of 4.11 for a slew rate of 3.0 and load capacitance of 0.4, in computing the power consumption of NAND circuit 40. It is apparent that the use of such a fixed value provides less precise computation of power consumption.

**[0020]** From IEEE TRANSACTIONS ON COMPUTER AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, vol. 9, no. 6, June 1990, NEW YORK US, pages 642 through 654, COWDHURY ET AL, "Estimation of Maximum Currents in MOS IC Logic Circuits" a method of current estimation for CMOS gates and CMOS macros is known. The estimation considers three components of the current to be estimated: a static current due to leakage, a current due to charging and discharging of load capacitance and a short-circuit current. It is further described that the maximum current depends on several factors, e.g., the input slew rate and the capacitances connected to various nodes of the gate. Further, only capacitances of the output-side of the gate are taken into account.

**[0021]** From 1989 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, May 8, 1989, PORTLAND OR US, pages 881 through 884, TJÄRNSTRÖM, "Power Dissipation Estimate by Switch Level Simulation" an apparatus for computing power consumption in a MOS transistor logic function block according to the preamble of claim 1 is known.

**[0022]** It is therefore an object of the present invention to provide a power consumption computing apparatus free of the above-described disadvantages, which can compute power consumption in a macrocell precisely.

**[0023]** According to the present invention, this object is solved by the advantageous measures indicated in the characterizing part of claim 1.

**[0024]** Further advantageous modifications of the present invention are subject matter of the subclaims.

**[0025]** According to a feature of the present invention, apparatus for computing power consumption in MOS transistor macrocell does not use a fixed value for power consumption caused by through-current, but computes power consumption with variations depending on a slope of input waveform and variations depending on operating points of MOS transistors as determined by output-side load capacitance.

**[0026]** Power consumption W of a macrocell is the sum of power consumption Wp caused by through-current and power consumption Wc caused by load capacitance. According to the present invention, the term of power consumption caused by through-current is determined by an input slew rate and output-side load. For determining through-current power consumption term, a computation expression expressed as a function f(t, c), where t is a slew rate and c is load capacitance, is used. In other words, according to the present invention, the term of power consumption caused by through-current is determined by an input slew rate and an output-side load.

**[0027]** In the drawings:

FIGURE 1 is a block diagram showing an arrangement of prior art macrocell power consumption computation apparatus;
FIGURE 2 is a block diagram showing a typical arrangement of apparatus for computing power consumption in a circuit;
FIGURE 3 is a circuit diagram of a macrocell;
FIGURE 4 is a block diagram of macrocell power consumption computation apparatus as an example for elucidating the present invention; and
Figure 5 is a block diagram of macrocell power consumption computation apparatus according to an embodiment of the present invention.

**[0028]** FIGURE 4 shows apparatus for computing power consumption in a macrocell for elucidating the present invention. The apparatus includes circuit information deriving means 21, slew rate determining means 25, a memory section 26 for storing a function f(t) for determining power consumption Wp caused by through-current, means 27 for determining through-current power consumption Wp, means 28 for determining power consumption Wc caused by load capacitance, and means 29 for summing Wp and Wc.

**[0029]** Circuit information deriving means 21 derives circuit information necessary for computing power consumption in each macrocell which exhibits signal changes in simulation, i.e. input and output load capacitance for each such macrocell, based on data 22 relating to input and output signal changes in a macrocell exhibited in logic simulation, a net list 23 containing the name of that macrocell and its circuit connection information, and load capacitance data 24 which represents capacitance itself or computation parameters corresponding to gate capacitance and drain capaci-

tance determined by characteristics of MOS transistors forming the macrocell, and capacitance provided by wires connecting that macrocell to other macrocells.

**[0030]** Slew rate determining means 25 determines a slew rate t of an input signal exhibiting signal changes at an input terminal of a macrocell of interest based on input-side capacitance information supplied from circuit information deriving means 21.

**[0031]** The term "slew rate" as used herein represents the time required for the input signal to change from 0V to 5V, for example, but usually, it represents such a time required for the input signal to change from 0.5V to 4.5V, i.e. the lower limit being raised by 10% of the range above and the upper limit being lowered by 10% of the range.

**[0032]** Wp determining function f(t) memory section 26 contains a number of computation expressions for respective types of macrocells used. Each of the expressions expresses the power consumption Wp caused by through-current by means of a function f(t) of a slew rate t (time) of each macrocell.

**[0033]** Means 27 for determining power consumption Wp caused by through-current reads out a computation expression for the macrocell of interest from Wp determining function memory section 26 and computes the power consumption Wp caused by through-current in the subject macrocell, using a slew rate provided by slew rate determining means 25.

**[0034]** Means 28 for determining the power consumption caused by load capacitance computes, based on information from circuit information deriving means 21, i.e. based on the derived output-side load capacitance of the subject macrocell, the power consumption Wc due to charging and discharging that capacitance. Means 28 computes the power consumption Wc, using a known computation expression for power consumption Wc caused by load capacitance.

**[0035]** Means 29 sums the Wp computed by Wp determining means 27 and Wc computed by Wc determining means 28 to produce the overall consumed power of the macrocell.

**[0036]** The arrangement shown in FIGURE 4 is similar to that shown in FIGURE 1, except that the arrangement of FIGURE 4 includes slew rate determining means 25, Wp determining function memory section 26, and Wp determining means 27.

**[0037]** The output of this arrangement shown in FIGURE 4 is applied to means corresponding to means 12 in the arrangement shown in FIGURE 2 to compute the overall power consumption of the circuit comprising the macrocells when the circuit is operating.

**[0038]** Since the power consumption Wp caused by through-current is a function of slew rate t, the computation of power consumption of this example takes into account changes of power consumption caused by changes of the slope of an input waveform, and, therefore, its computation precision is higher than that of conventional techniques described above in which a fixed value is used for the term for power consumption caused by through-current in the computation expression. For instance, for the same macrocell (NAND circuit) used in the explanation of TABLE 1, the power consumption which changes with change in slew rate is shown in TABLE 2, which is obtained by using a computation expression,

$$Wp = 0.840 + 0.123t$$

TABLE 2

| Load \ Slew Rate | 1.0 | 2.0 | 3.0 | 4.0 | 5.0 |
|---|---|---|---|---|---|
| 0.2 | 1.96 | 3.09 | 4.21 | 5.33 | 6.46 |
| 0.4 | 1.96 | 3.09 | 4.21 | 5.33 | 6.46 |
| 0.6 | 1.96 | 3.09 | 4.21 | 5.33 | 6.46 |

**[0039]** The results shown in TABLE 2 are very close to the actual power consumption shown in TABLE 1, and are much more precise than results which would obtained by using a fixed value for power consumption caused by through-current. The values shown in TABLE 2 do not change with change in load capacitance, but, depending on types of macrocells, computation precision is sufficiently improved.

**[0040]** FIGURE 5 is a block diagram of macrocell power consumption computation apparatus according to an embodiment of the present invention. The difference from the apparatus shown in FIGURE 4 is that in place of memory section 26 which stores Wp determining function f(t) and Wp determining means 27, a memory section 30 for storing a Wp determining function f(t,c) and Wp determining means 31 are used.

**[0041]** Wp determining function memory section 30 stores therein a number of computation expressions for various types of macrocells. Computation expressions are in the form of a function f(t,c) for determining power consumption Wp as a function of a slew rate t and load capacitance c of a macrocell.

**[0042]** The remainder of the apparatus is same as the apparatus of FIGURE 4, and, therefore, no further explanation is necessary. The output of the power consumption computation apparatus of FIGURE 5 is also applied to means corresponding means 12 of FIGURE 2 for determining the power consumption of a circuit when the circuit is operating.

**[0043]** In this embodiment, the expression for use in computing power consumption Wp caused by through-current is in the form of a function of slew rate t and load capacitance c. In the computation apparatus of this embodiment, changes in power consumption due to changes in slew rate t and load capacitance c are taken into account. In other words, changes in power consumption depending on changes in slope of the input waveform and depending on changes in operating point of MOS transistors caused by output-side load are taken into account. This significantly improves the precision of computation relative to prior art in which a fixed value is used for power consumption caused by through-current. For example, for the same macrocell (NAND circuit) used in explaining TABLE 1, the following computation expression may be used to obtain the results shown in TABLE 3.

$$Wp = 0.834 + 1.291t + 0.394tc$$

TABLE 3 shows power consumption of the macrocell which varies with the slew rate t and the load capacitance c.

TABLE 3

| Load \ Slew Rate | 1.0 | 2.0 | 3.0 | 4.0 | 5.0 |
|---|---|---|---|---|---|
| 0.2 | 2.05 | 3.26 | 4.47 | 5.68 | 6.89 |
| 0.4 | 1.97 | 3.10 | 4.23 | 5.37 | 6.50 |
| 0.6 | 1.89 | 2.94 | 4.00 | 5.05 | 6.11 |

**[0044]** As is seen, the values obtained as shown in TABLE 3 are very close to the actual values shown in TABLE 1, which means that the apparatus shown in FIGURE 5 can provide highly precise results relative to prior art in which a fixed value is used for power consumption caused by through-current, because the computation takes into account a slew rate t and load capacitance c, significant improvement in computation precision can be achieved.

**[0045]** The load capacitance c used in this embodiment is the same as the information used in computing power consumption due to load capacitance, and, therefore, the same information as used for computing Wc can be used. Accordingly, realization of this embodiment is easy.

**[0046]** In the example of FIGURE 4, the expression $Wp=\alpha + \beta t$ was used, and in the embodiment, the expression $Wp= \alpha + \beta t - \gamma tc$ was used, where $\alpha$, $\beta$ and $\gamma$ are constants. However, other computation expression may be used instead.

## Claims

1. Apparatus for computing power consumption in an MOS transistor logic function block, comprising:

   circuit information deriving means (21) for deriving circuit information appropriate for a logic function block of interest based on input and output varying signals to and from said logic function block and a net list (23);

slew rate determining means (25) for determining an input slew rate based on information from said circuit information deriving means (21);

a memory section (30) containing expressions for use in computation of power consumption caused by through-current, each expression corresponding to a different one of various types of logic function blocks and representing power consumption caused by through-current as a function of a slew rate; and

means (31) for determining power consumption due to through-current by substituting the slew rate as determined by said slew rate determining means (25) into the computation expression as read from said memory section (30),

*characterized in that*

said circuit information deriving means (21) derives circuit information appropriate for a logic function block of interest also based on output-load capacitance data; and

said means (31) for determining power consumption due to through current also substitutes the output-load capacitance data into the computation expression as read from said memory section (30).

2. Apparatus for computing power consumption in an MOS transistor logic function block according to claim 1, *characterized by:*

means (28) for determining power consumption caused by load capacitance; and

means (29) for summing the power consumption as determined by said means (31) for determining power consumption caused by through-current and the power consumption as determined by said means (28) for determining power consumption caused by load capacitance.

3. Apparatus for computing power consumption in an MOS transistor logic function block according to claim 2, *characterized by* means for multiplying power consumption in one cycle of each logic function block by a number of operating cycles in unit time, and summing the results of respective logic function blocks.

**Patentansprüche**

1. Vorrichtung zum Berechnen einer Leistungsaufnahme eines MOS-Transistor-Logikfunktionsblock, die aufweist:

eine Einrichtung (21) zum Ableiten einer Schaltungsinformation, die eine Schaltungsinformation, die für einen Logikfunktionsblock von Interesse zweckmäßig ist, auf der Grundlage von sich ändernden Eingangs- und Ausgangsignalen in und aus dem Logikfunktionsblock und einer Netzliste (23) ableitet;

eine Einrichtung (25) zum Bestimmen einer Eingangsanstiegsgeschwindigkeit, die eine Eingangsanstiegsgeschwindigkeit auf der Grundlage einer Information aus der Einrichtung (21) zum Ableiten einer Schaltungsinformation bestimmt;

einen Speicherbereich (30), der Ausdrücke zur Verwendung bei einer Berechnung einer Leistungsaufnahme enthält, die durch einen Durchgangsstrom verursacht wird, wobei jeder Ausdruck einem unterschiedlichen von verschiedenen Typen von Logikfunktionsblöcken entspricht und eine Leistungsaufnahme, die durch einen Durchgangsstrom verursacht wird, als eine Funktion einer Anstiegsgeschwindigkeit darstellt; und

eine Einrichtung (31) zum Bestimmen einer Leistungsaufnahme aufgrund eines Durchgangsstroms durch Einsetzen der Anstiegsgeschwindigkeit, wie sie von der Einrichtung (25) zum Bestimmen einer Anstiegsgeschwindigkeit bestimmt wird, in den Berechnungsausdruck, wie er aus dem Speicherbereich (30) gelesen wird,

*dadurch gekennzeichnet, daß*

die Einrichtung (21) zum Ableiten einer Schaltungsinformation eine Schaltungsinformation, die für einen Logikfunktionsblock von Interesse zweckmäßig ist, ebenso auf der Grundlage von Ausgangslastkapazitätsdaten

ableitet; und

die Einrichtung (31) zum Bestimmen einer Leistungsaufnahme aufgrund eines Durchgangsstroms ebenso die Ausgangslastkapazitätsdaten in den Berechnungsausdruck einsetzt, wie er aus dem Speicherbereich (30) gelesen wird.

2. Vorrichtung zum Berechnen einer Leistungsaufnahme in einem MOS-Transistor-Logikfunktionsblock nach Anspruch 1, *gekennzeichnet durch:*

eine Einrichtung (28) zum Bestimmen einer Leistungsaufnahme, die durch eine Lastkapazität bestimmt wird; und

eine Einrichtung (29) zum Summieren der Leistungsaufnahme, wie sie von der Einrichtung (31) zum Bestimmen einer Leistungsaufnahme bestimmt wird, die durch einen Durchgangsstrom verursacht wird, und der Leistungsaufnahme, wie sie von der Einrichtung (28) zum Bestimmen einer Leistungsaufnahme bestimmt wird, die durch eine Lastkapazität verursacht wird.

3. Vorrichtung zum Berechnen einer Leistungsaufnahme in einem MOS-Transistor-Logikfunktionsblock nach Anspruch 2, *gekennzeichnet durch* eine Einrichtung zum Multiplizieren einer Leistungsaufnahme in einem Zyklus jedes Logikfunktionsblocks mit einer Anzahl von Betriebszyklen in einer Einheitszeit und zum Summieren der Ergebnisse von jeweiligen Logikfunktionsblöcken.

**Revendications**

1. Dispositif pour calculer la consommation de puissance dans un bloc de fonction logique à transistors MOS, comprenant:

des moyens d'obtention d'information de circuit (21) pour obtenir une information de circuit appropriée pour un bloc de fonction logique considéré, sur la base de signaux variables d'entrée et de sortie du bloc de fonction logique, et d'une liste de réseau (23);
des moyens de détermination de vitesse de balayage (25) pour déterminer une vitesse de balayage d'entrée basée sur l'information provenant des moyens d'obtention d'information de circuit (21);
une section de mémoire (30) contenant des expressions pour l'utilisation dans le calcul de la consommation de puissance qui est occasionnée par le courant traversant, chaque expression correspondant à l'un différent de divers types de blocs de fonction logique, et représentant la consommation de puissance qui est occasionnée par le courant traversant, en fonction d'une vitesse de balayage; et
des moyens (31) pour déterminer la consommation de puissance qui est due au courant traversant, en substituant dans l'expression de calcul qui est lue dans la section de mémoire (30), la vitesse de balayage qui est déterminée par les moyens de détermination de vitesse de balayage (25),

caractérisé en ce que

les moyens d'obtention d'information de circuit (21) obtiennent une information de circuit appropriée pour un bloc de fonction logique considéré, en se basant également sur des données de capacité de charge de sortie; et les moyens (31) pour déterminer la consommation de puissance qui est due au courant traversant substituent également dans l'expression de calcul qui est lue dans la section de mémoire (30) les données de capacité de charge de sortie.

2. Dispositif pour calculer la consommation de puissance dans un bloc de fonction logique à transistors MOS selon la revendication 1, caractérisé par:

des moyens (28) pour déterminer la consommation de puissance qui est occasionnée par une capacité de charge; et
des moyens (29) pour faire la somme de la consommation de puissance qui est déterminée par les moyens (31) pour déterminer la consommation de puissance occasionnée par le courant traversant, et de la consommation de puissance qui est déterminée par les moyens (28) pour déterminer la consommation de puissance qui est occasionnée par la capacité de charge.

3. Dispositif pour calculer la consommation de puissance dans un bloc de fonction logique à transistors MOS selon la revendication 2, caractérisé par des moyens pour multiplier la consommation de puissance dans un cycle de chaque bloc de fonction logique, par un nombre de cycles de fonctionnement par unité de temps, et pour faire la somme des résultats de blocs de fonction logique respectifs.

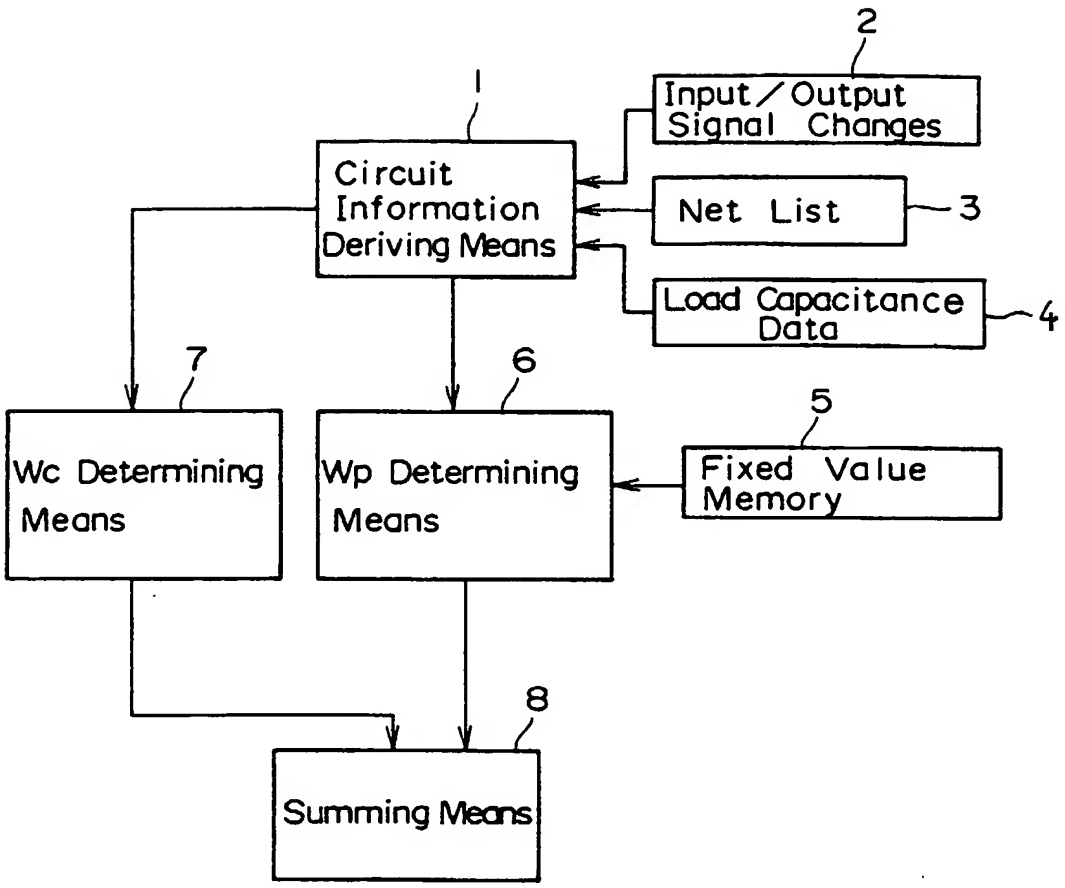



Fig. 1 Prior Art

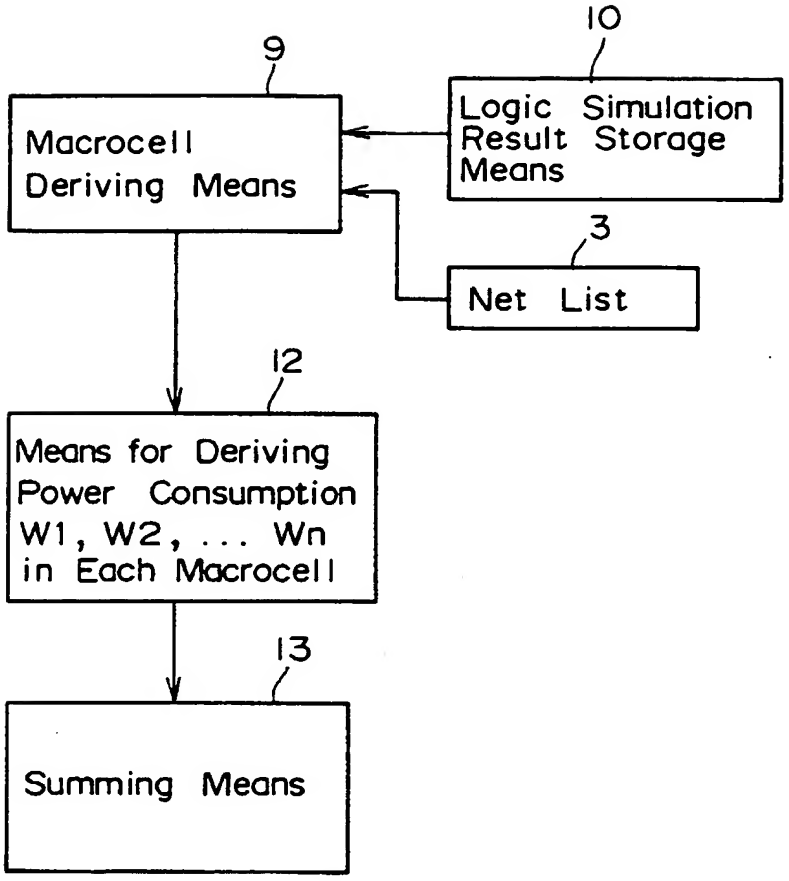

9
10
Macrocell Deriving Means
Logic Simulation Result Storage Means
3
Net List
12
Means for Deriving Power Consumption W1, W2, ... Wn in Each Macrocell
13
Summing Means

Fig. 2

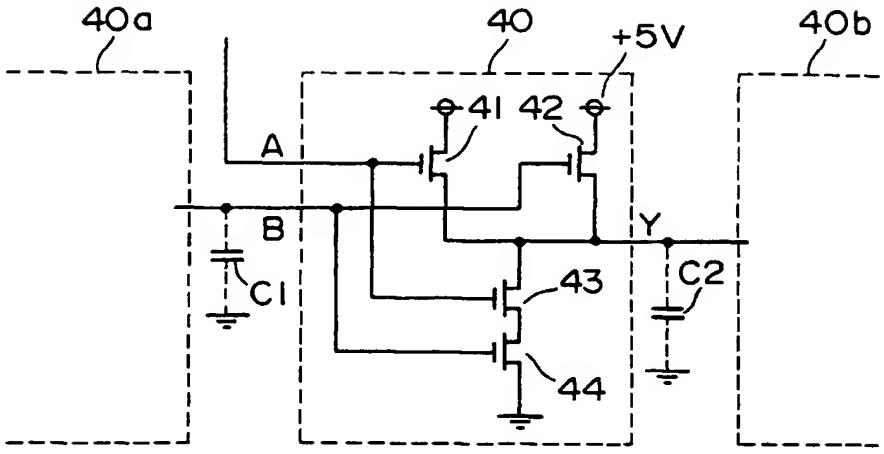



Fig. 3

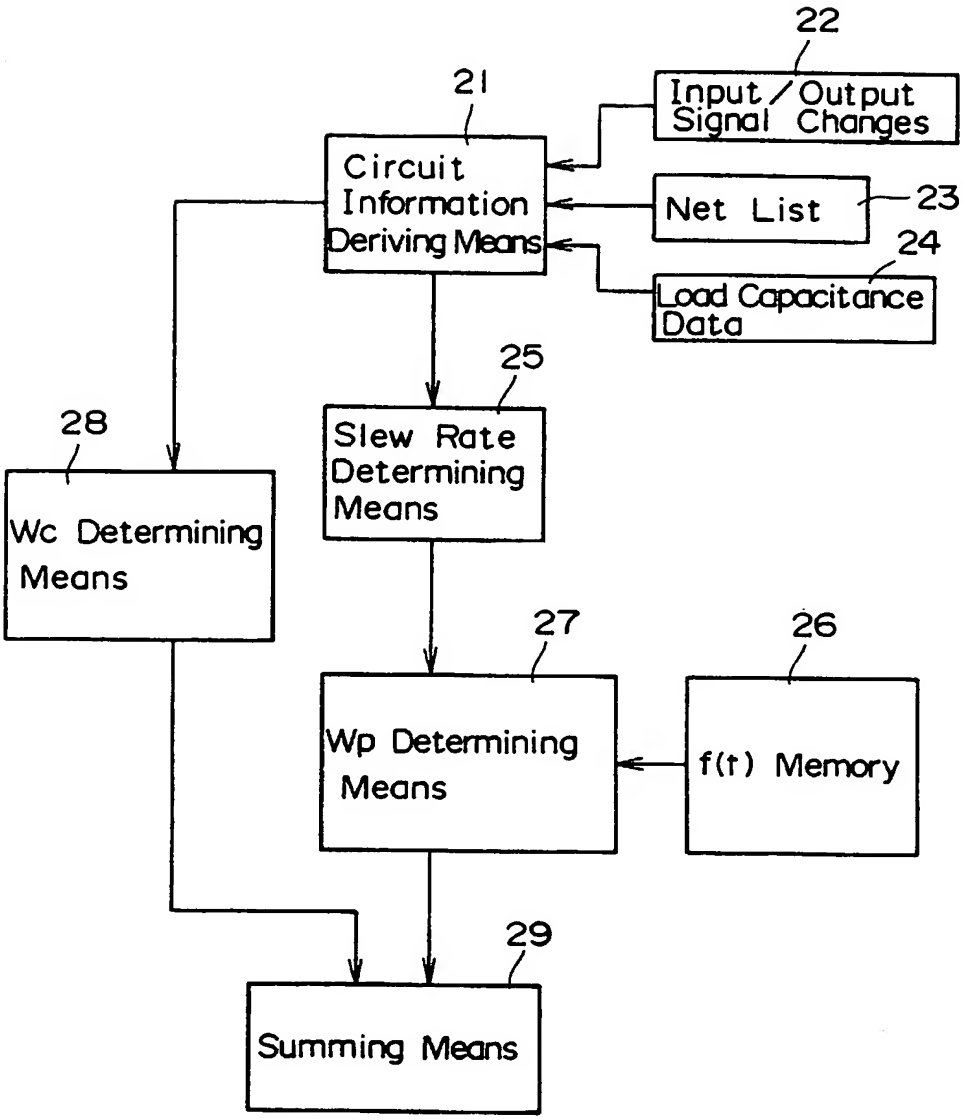
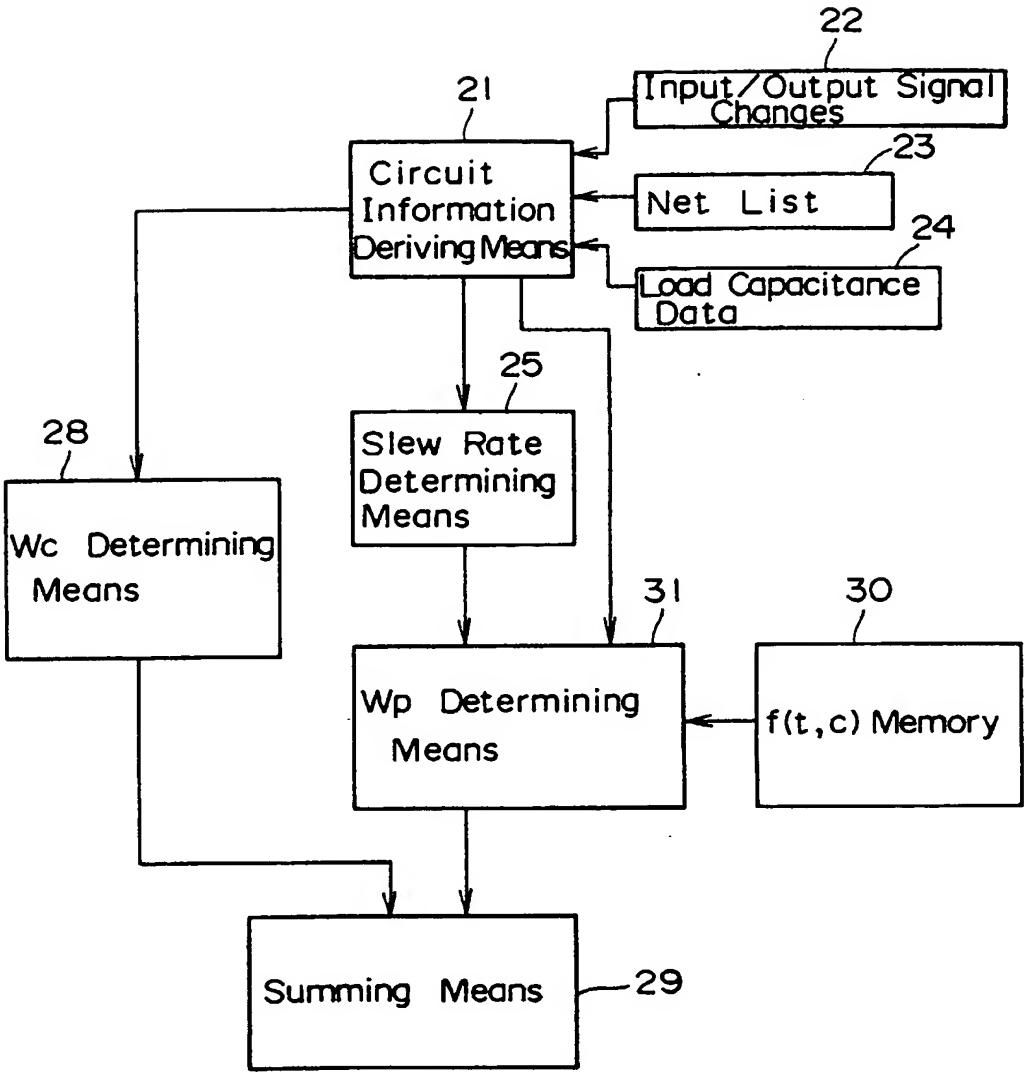

22
21
Input / Output Signal Changes
Circuit Information Deriving Means
Net List
23
24
Load Capacitance Data
25
28
Slew Rate Determining Means
Wc Determining Means
27
26
Wp Determining Means
f(t) Memory
29
Summing Means

Fig. 4


22
Input/Output Signal Changes
21
Circuit Information Deriving Means
23
Net List
24
Load Capacitance Data
25
Slew Rate Determining Means
28
Wc Determining Means
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30
Wp Determining Means
f(t,c) Memory
Summing Means
29

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